LIBRARY ieee;

USE ieee.std\_logic\_1164.all;

ENTITY lab8 IS

PORT( Clock, Rstn, Enable :IN STD\_LOGIC;

Count :OUT STD\_LOGIC\_VECTOR(1 DOWNTO 0));

END lab8;

ARCHITECTURE Behavior OF lab8 IS

TYPE State\_type IS(A,B,C,D);

SIGNAL y : State\_type;

BEGIN

PROCESS(Rstn,Clock)

BEGIN

IF Rstn ='0' THEN

Count <= "00";

y <= A;

ELSIF (Clock'EVENT AND Clock = '1') THEN

CASE y IS

WHEN A=>

IF Enable = '0' THEN

Count <= "00";

y <= A;

ELSE

Count <= "01";

y <= B;

END IF;

WHEN B=>

IF Enable = '0' THEN

Count <= "01";

y <= B;

ELSE

Count <= "10";

y <= C;

END IF;

WHEN C=>

IF Enable = '0' THEN

Count <= "10";

y <= C;

ELSE

Count <= "11";

y <= D;

END IF;

WHEN D=>

IF Enable = '0' THEN

Count <= "11";

y <= D;

ELSE

Count <= "00";

y <= A;

END IF;

END CASE;

END IF;

END PROCESS;

END Behavior;